WHAT IS CLAIMED IS:

1. A method of testing a clock and data recovery device (CDR), comprising:
producing test data from a first CDR; and
testing another second CDR based on the test data from the first CDR.

2. The method of claim 1, further comprising:
outputting the test data based on a clock; and
generating data drift in the test data by changing a phase of the clock.

3. The method of claim 2, further comprising:
setting the phase of the clock based on a count value; and
changing the count value across a range of phase shifts.

4. The method of claim 3, further comprising:
incrementing/decrementing the count value until a maximum/minimum count value is reached;
subsequently decrementing/incrementing the count value until a minimum/maximum count value is reached; and
repeating the above steps until all the test data is generated.

5. The method of claim 4, further comprising:
adding one or more least significant bits to the counter value;
incrementing/decrementing added least significant bits when incrementing/decrementing the counter value.

6. The method of claim 2, further comprising:
generating test data results in the second CDR device; and
verifying the test data results.

7. The method of claim 1, further comprising:
producing test data from the second CDR; and
testing the first CDR based on the test data from the second CDR.

8. A method of testing a plurality of clock and data recovery devices (CDRs), comprising:

initializing one CDR to generate test data using a test data generator of the one CDR;

initializing remaining CDRs to receive the test data;

applying the test data to the remaining CDRs using the test data generator of the one CDR; and

producing data drift in the test data by changing a phase of a clock that is applied to the test data generator.

9. A method of testing a plurality of clock and data recovery devices (CDRs), comprising:

initializing a first CDR to generate a first test data using a first test data generator of the first CDR;

initializing a second CDR to receive the first test data;

applying the first test data to the second CDR using the first test data generator of the first CDR;

producing a first data drift in the first test data by changing a phase of a first clock that is applied to the first test data generator;

initializing the second CDR to generate a second test data using a second test data generator of the second CDR, if a test of the second CDR is completed;

initializing the first CDR to receive the second test data;

applying the second test data to the first CDR using the second test data generator of the second CDR; and

producing a second data drift in the second test data by changing a phase of a second clock that is applied to the second test data generator.

10. A clock and data recovery device (CDR) device, comprising:

a phase variable clock source to generate a phase variable clock;

a test data generator to generate test data based on the phase variable clock;

a counter that has a count value to control a phase of the phase variable clock; and

a finite state machine to increment/decrement the count value.

11. The CDR of claim 10, wherein the finite state machine

increments/decrements the count value until a maximum/minimum count value is reached, and

subsequently decrements/increments the count value until a minimum/maximum count value is reached, wherein the finite machine increments/decrements the count value until all the test data is generated.

12. The CDR of claim 11, wherein:

the counter includes one or more least significant bits added to the counter value, the counter without the least significant bits are used to control the phase of the phase variable clock; and

the finite state machine increments/decrements the least significant value bits when incrementing/decrementing the counter value.

13. The CDR of claim 10, wherein the test data generator is a pseudo random number generator.

14. The CDR of claim 10, wherein the phase variable clock source is a phase rotator coupled to a phase locked loop (PLL) oscillator.

15. A system or a network implementing the CDR of claim 10.

16. A clock and data recovery device (CDR) device to test another second CDR, comprising:

means for generating test data to test the second CDR; and

means for producing a range of data drift conditions in the test data.

17. The CDR of claim 16, wherein means for producing a range of data drift conditions include means for reducing a rate of data drift.

18. An apparatus including a plurality of clock and data recovery devices, comprising:

a first CDR having a test data generator; and

another second CDR, wherein the first CDR uses the test data generator to generate test data to test the second CDR.

19. The apparatus of claim 18, further comprising:
the first CDR having a finite state machine to adjust data drift in the test data.

20. The apparatus of claim 18, further comprising:
the second CDR having a data checker to check a test data result output.